REMARKS

Applicant gratefully acknowledge the allowance of claims 22-27. Claims 1, 5, 7, 9, 13, 17, 28-31 and 33-45 have been amended. Claims 1-45 remain pending in this application. Applicant reserves the right to pursue the original and any other claims in this and other applications.

Claims 1-21, 28-34 and 36-45 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Roth (U.S. Patent No. 6,771,525). The rejection is respectfully traversed.

Claim 1 recites a content addressable memory (CAM) comprising "match combining circuitry providing P/Q combined match signals, [where] each combined match signal [indicates] a combination of a group of Q match signals." Claim 1 further recites priority encoder circuitry that provides "P/Q priority signals indicating at most one combined match signal that has priority and is asserted."

Roth generally refers to a CAM that selectively combines match line latch outputs from two adjacent CAM memory arrays and provides the combined outputs to a multiple match resolver/priority encoder in response to a variable word width control signal. In particular, as described in the pending Office Action, Roth simply refers to combining match line outputs as the results of a search and comparison operation. The claimed invention, on the other hand, logically combines groups of Q match signals and thus, obtains P/Q combined match signals that depend on a search width indicated by bit length. This is a patentable distinctive result from that of Roth.

Specifically, the CAM of the claimed invention relates to "match combining circuitry that responds . . . to a signal indicating a search width that is a multiple of the location width," and provides "P/Q combined match signals, . . . the combination depending on the indicated search width." Moreover, the claimed invention relates to

"priority encoder circuitry that . . . [provides] P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion."

Applicant respectfully submits that Roth, as mentioned above, may generally refer to CAM combining circuitry and a priority encoder, however, Roth does not disclose, teach or suggest combining groups of Q match signals to obtain P/Q combined match signals. For at least the reasons set forth above, Applicant respectfully submits that Roth does not anticipate all limitations of the claim 1 invention.

Independent claims 5, 9, 13, 20, 28, 36, 38, 40, 41 and 43 recite limitations similar to the "priority encoder circuitry" discussed above. Independent claims 17, 31, 32, 34, 39 and 44 recite limitations similar to the "match combining circuitry" described above. Independent claims 7, 29, 34 and 37 recite limitations similar to both the "priority encoder circuitry" and "match combining circuitry" described above. For at least the reasons set forth above, all independent claims should be allowable. Claims 2-4 depend from claim 1 and should be allowable along with claim 1. Claim 6 depends from claim 5 and should be allowable along with claim 5. Claim 8 depends from claim 7 and should be allowable along with claim 7. Claims 10-12 depend from claim 9 and should be allowable along with claim 9. Claims 14-16 depend from claim 13 and should be allowable along with claim 13. Claims 18 and 19 depend from claim 17 and should be allowable along with claim 17. Claim 21 depends from claim 20 and should be allowable along with claim 20.

Accordingly, Applicant respectfully requests that the rejection be withdrawn and claims 1-21, 28-34 and 36-45 be allowed.

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Roth in view Ichiriu (U.S. Patent No. 6,901,000). The rejection is respectfully traversed.

Claim 35 recites similar limitations as recited above relating to claim 1. That is, claim 35 recites a CAM comprising "match combining circuitry that responds . . . to a signal indicating a search width that is a multiple of the location width," and provides "P/Q combined match signals, . . . the combination depending on the indicated search width," and "priority encoder circuitry that . . . [provides] P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion." As set forth above, Roth fails to disclose, teach or suggest these limitations.

The Office Action seeks to overcome the shortcomings of Roth by combining it with Ichiriu. The Office Action cites Ichiriu as teaching lower and upper address encoding circuitry. (Office Action at 6). However, Applicant respectfully submits that Ichiriu does not cure the shortcomings of Roth. Specifically, Ichiriu, which only shows an address comparand having encoding circuitry for even and odd registries, does not teach or suggest the above limitations.

Therefore, the cited combination fails to teach or suggest all limitations of the claimed invention, and thus does not render claim 35 obvious. Accordingly, Applicant respectfully requests that the rejection be withdrawn and claim 35 allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

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Respectfully submitted,

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